FIG. 1

FIFO MEMORY

WRITE ADDRESS 16   READ DATA 22

WRITE CLOCK 18   READ CLOCK 24

WRITE DATA 14   READ ADDRESS 26

WRITE ENABLE 20   READ ENABLE 28

FIFO USAGE

4X SYSTEM CLOCK

SYSTEM CLOCK GENERATOR

ENABLED

FIFO USAGE

CLOCK ENABLE

CLOCK

FIFO ADJUST LOGIC

COUNT

CLOCK ENABLE   CLOCK

MULTI-BIT COUNTER FOR READ ADDRESS

If Fifo Usage = OK

               !FifoAdjustSequnce

if Fifo Usage = Empty or Almost Empty

         Start FifoAdjust Sequence &

                       Repeat

if Fifo Usage = Full or Almost Full

            Start FifoAdjustSequence &

                       Drop

If !FifoAdjustSequence

         Clock Enable every 4th clock cycle

If FifoAdjustSequence & Drop

         Clock Enable after 3rd clock cycle

If FifoAdjustSequence & Repeat

         Clock Enable after 5th clock cycle

Note FifoAdjustSequence drop 4 1/4samples
over a period of time.

FIG. 2

READ DATA (e)   NO SAMPLES ARE SKIPPED OR REPEATED

READ DATA (a)   ONE SAMPLE IS SKIPPED   SAMPLE SKIPPED

FIG. 3

READ DATA (a)   ONE SAMPLE IS REPEATED   SAMPLE REPEATED

FIG. 4

JITTER CAUSED BY SKIPPING ONE SAMPLE (ONE CLOCK CYCLE)

JITTER CAUSED BY REPEATING ONE SAMPLE (ONE CLOCK CYCLE)

1/4 SAMPLE SKIPPED

ONE QUARTER SAMPLE IS SKIPPED

1/4 SAMPLE REPEATED

FIG. 5

READ DATA (d) ONE QUARTER SAMPLE IS REPEATED
READ ADDRESS (e)

JITTER CAUSED BY SKIPPING ONE QUARTER SAMPLE (1/4 CLOCK CYCLE)

JITTER CAUSED BY REPEATING ONE QUARTER SAMPLE (1/4 CLOCK CYCLE)